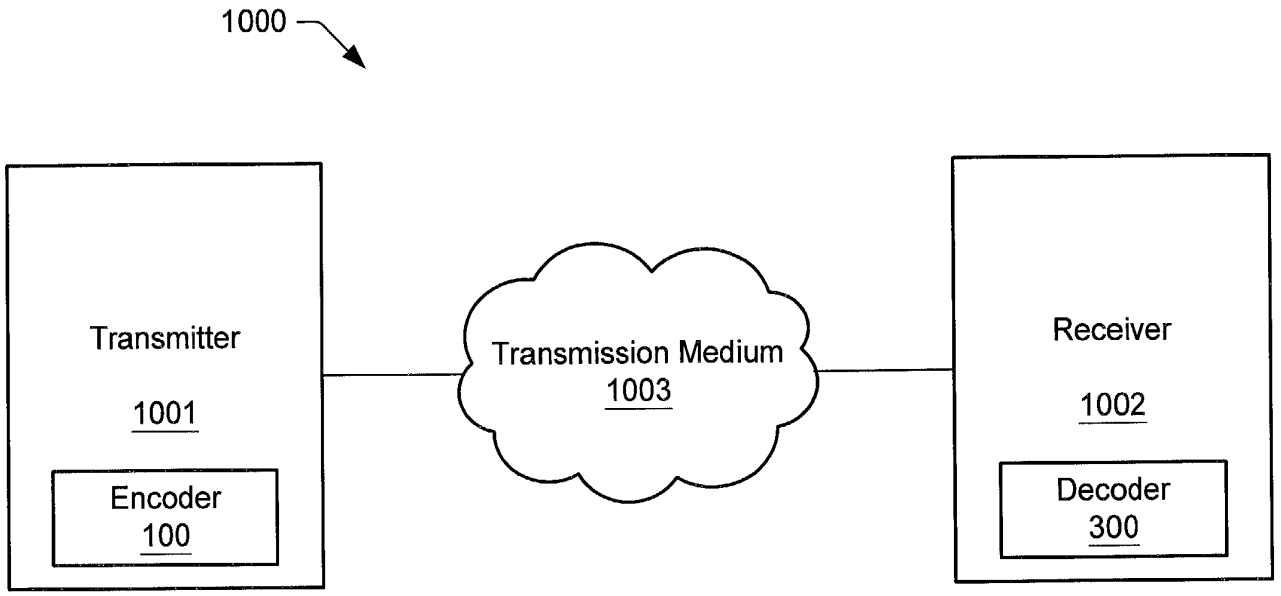

1000
Transmitter
1001
Encoder
100
Transmission Medium
1003
Receiver
1002
Decoder
300

FIG. 1

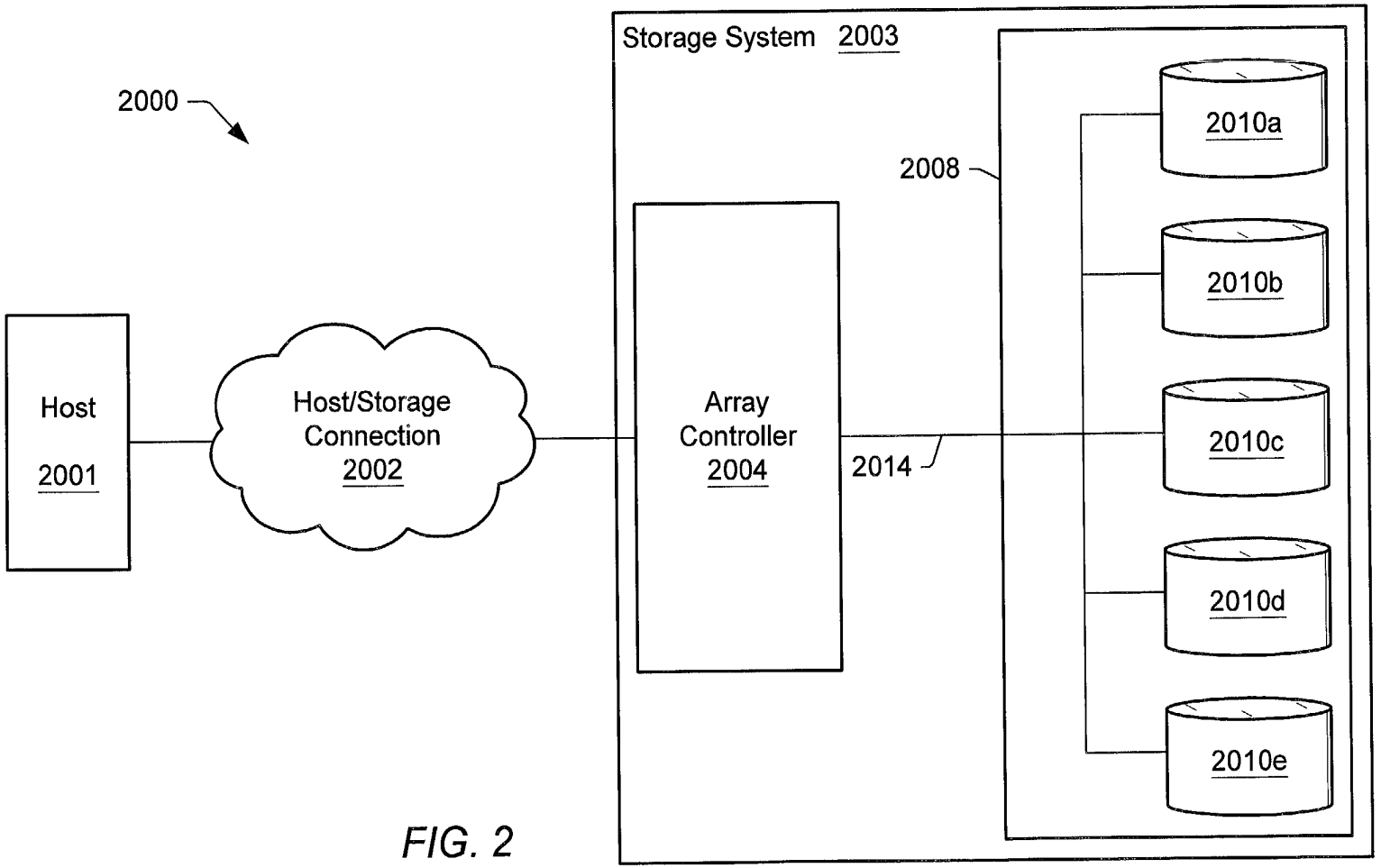

2000
Storage System 2003
2008
2010a
2010b
2010c
2010d
2010e
Host
2001
Host/Storage
Connection
2002
Array
Controller
2004
2014

FIG. 2

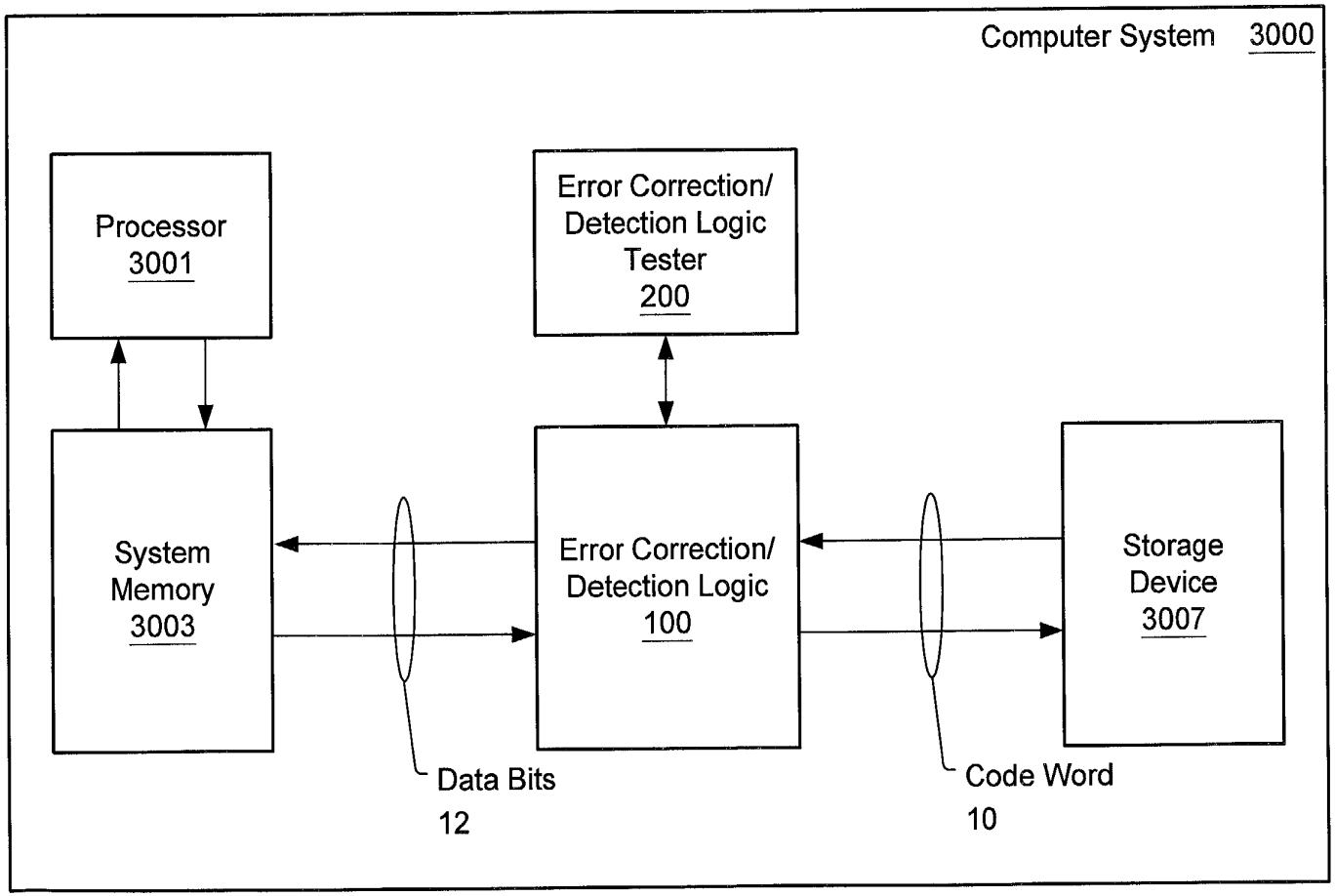

Computer System 3000
Processor 3001
Error Correction/ Detection Logic Tester 200
System Memory 3003
Error Correction/ Detection Logic 100
Storage Device 3007
Data Bits 12
Code Word 10

FIG. 3

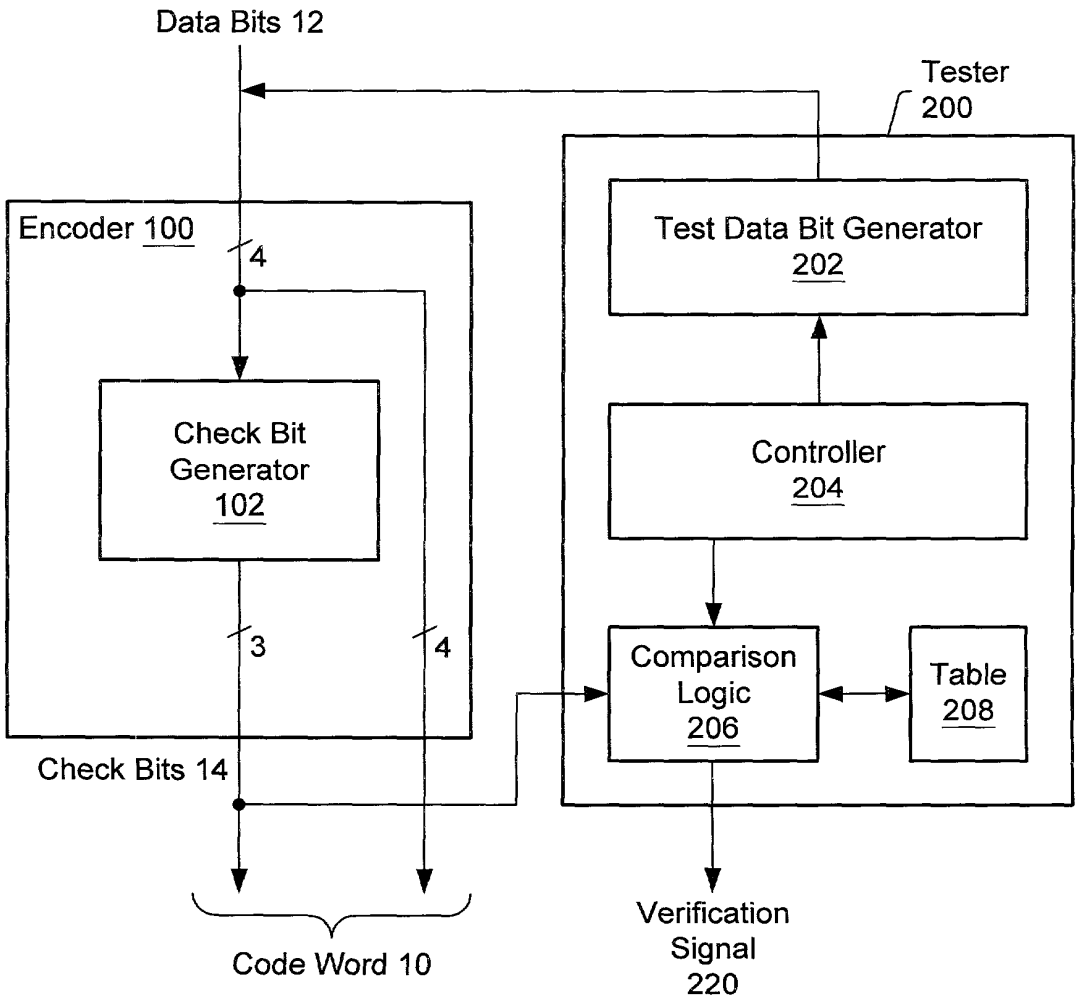
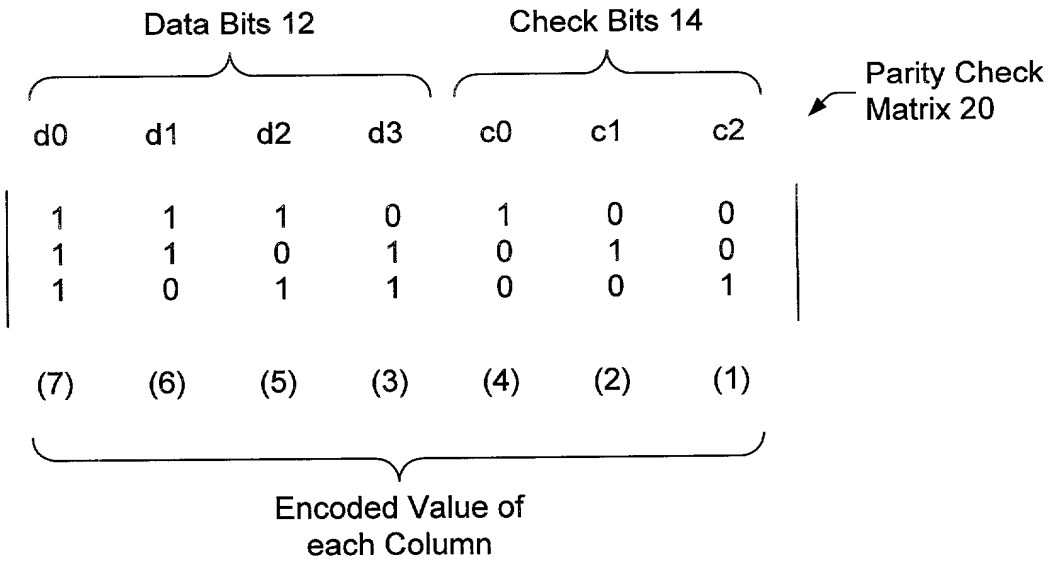

Data Bits 12
Tester
200
Encoder 100
4
Test Data Bit Generator
202
Check Bit
Generator
102
Controller
204
3
4
Comparison
Logic
206
Table
208
Check Bits 14
Code Word 10
Verification
Signal
220

FIG. 4A



Check Bit Equations 22

c0 = d0 XOR d1 XOR d2
c1 = d0 XOR d1 XOR d3
c2 = d0 XOR d2 XOR d3

FIG. 4B

Data Bits 12				Check Bits 14		
d0	d1	d2	d3	c0	c1	c2
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	1	0	1
0	0	1	1	1	1	0
0	1	0	0	1	1	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	0	0
1	1	1	1	1	1	1

Table 30

FIG. 4C

Data Bits 12 | Check Bits 14 ← Table 40A

d0	d1	d2	d3	c0	c1	c2
0	0	0	1	0	1	1
0	0	1	0	1	0	1
0	1	0	0	1	1	0
1	0	0	0	1	1	1

FIG. 4D

Data Bits 12 | Check Bits 14 ← Table 40B

d0	d1	d2	d3	c0	c1	c2
0	1	1	1	0	0	0
1	0	1	1	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	0	0

FIG. 4E

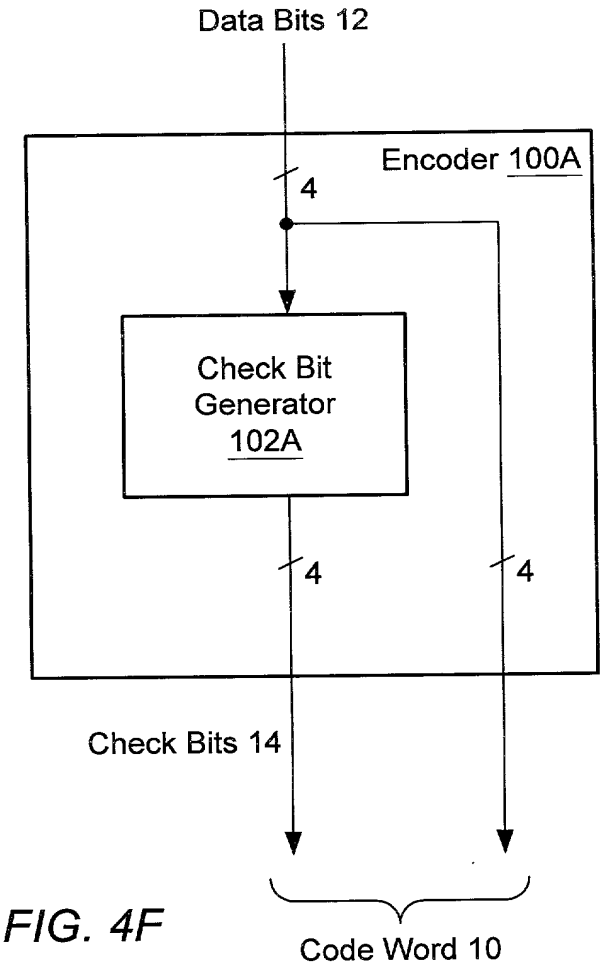
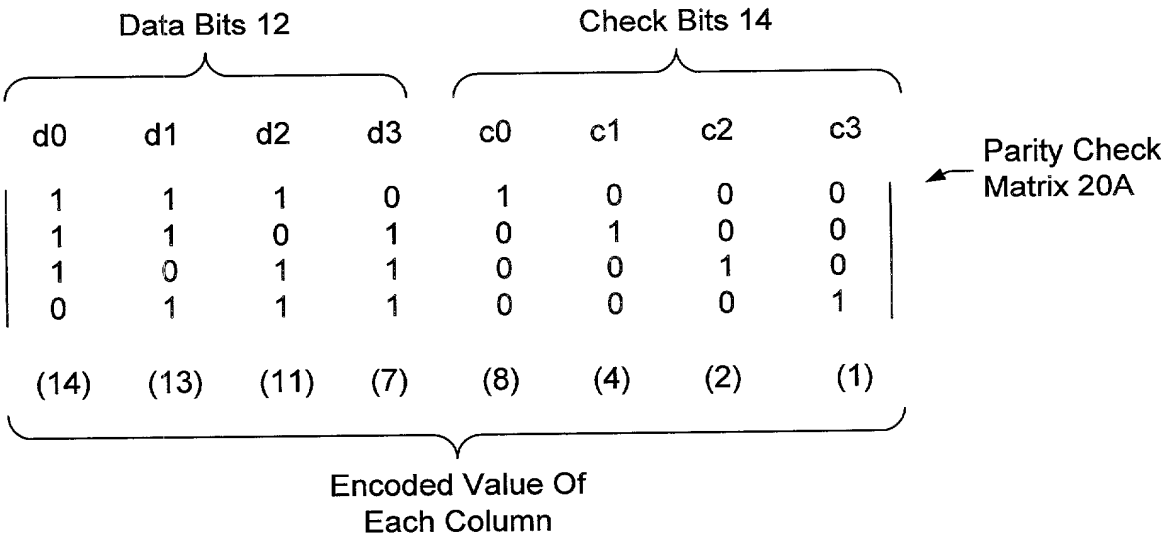

Data Bits 12
Encoder 100A
4
Check Bit Generator 102A
4
4
Check Bits 14
Code Word 10

FIG. 4F



Check Bit Equations 22A

c0 = d0 XOR d1 XOR d2
c1 = d0 XOR d1 XOR d3
c2 = d0 XOR d2 XOR d3
c3 = d1 XOR d2 XOR d3

FIG. 4G

Table 30A

Data Bits 12				Check Bits 14			
d0	d1	d2	d3	c0	c1	c2	c3
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
0	1	1	1	0	0	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	1	1
1	1	0	1	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	1

FIG. 4H

Table 40C

Data Bits 12				Check Bits 14			
d0	d1	d2	d3	c0	c1	c2	c3
0	0	0	1	0	1	1	1
0	0	1	0	1	0	1	1
0	1	0	0	1	1	0	1
1	0	0	0	1	1	1	0

FIG. 4I

Table 40D

Data Bits 12				Check Bits 14			
d0	d1	d2	d3	c0	c1	c2	c3
0	1	1	1	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	1	0	1	0	0
1	1	1	0	1	0	0	0

FIG. 4J

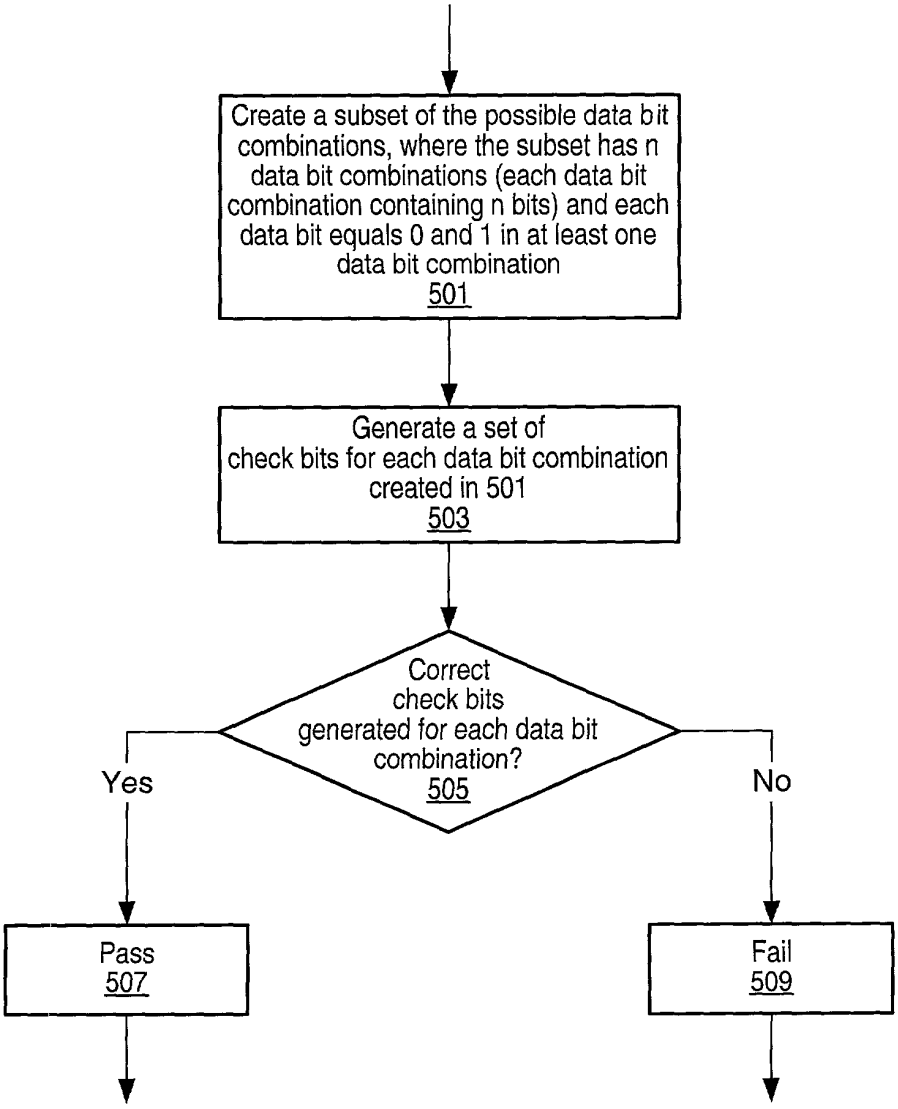

Create a subset of the possible data bit combinations, where the subset has n data bit combinations (each data bit combination containing n bits) and each data bit equals 0 and 1 in at least one data bit combination
501
Generate a set of check bits for each data bit combination created in 501
503
Correct check bits generated for each data bit combination?
505
Yes
No
Pass
507
Fail
509

FIG. 5

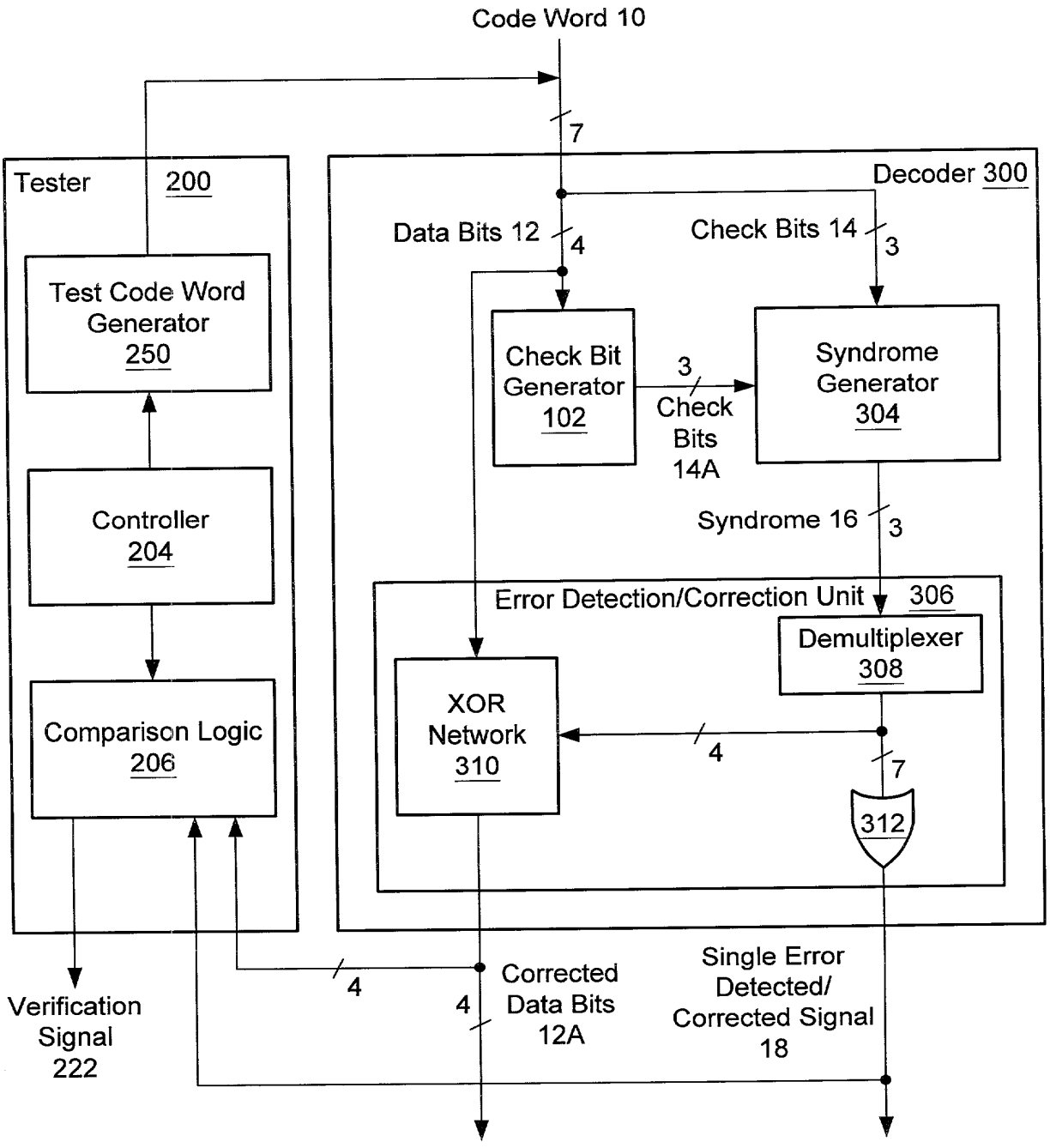

Code Word 10
7
Tester 200
Decoder 300
Data Bits 12
4
Check Bits 14
3
Test Code Word Generator 250
Check Bit Generator 102
3
Check Bits 14A
Syndrome Generator 304
Controller 204
Syndrome 16
3
Error Detection/Correction Unit 306
Demultiplexer 308
XOR Network 310
4
7
312
Comparison Logic 206
Verification Signal 222
4
4
Corrected Data Bits 12A
Single Error Detected/ Corrected Signal 18

FIG. 6A

Regenerated Check Bit Equations 22A

new c0 = d0 XOR d1 XOR d2
new c1 = d0 XOR d1 XOR d3
new c2 = d0 XOR d2 XOR d3

Syndrome Equations 24

s0 = c0 XOR new c0
s1 = c1 XOR new c1
s2 = c2 XOR new c2

Table 50A

	Code Word 10							Syndrome 18		
Error	d0	d1	d2	d3	c0	c1	c2	s0	s1	s2
none	0	0	0	0	0	0	0	0	0	0
c2	0	0	0	0	0	0	1	0	0	1
c1	0	0	0	0	0	1	0	0	1	0
c0	0	0	0	0	1	0	0	1	0	0
d3	0	0	0	1	0	0	0	0	1	1
d2	0	0	1	0	0	0	0	1	0	1
d1	0	1	0	0	0	0	0	1	1	0
d0	1	0	0	0	0	0	0	1	1	1

FIG. 6B

Regenerated Check Bit Equations 22A

new c0 = d0 XOR d1 XOR d2
new c1 = d0 XOR d1 XOR d3
new c2 = d0 XOR d2 XOR d3
new c3 = d1 XOR d2 XOR d3

Syndrome Equations 24

s0 = c0 XOR new c0
s1 = c1 XOR new c1
s2 = c2 XOR new c2
s3 = c3 XOR new c3

Table 50B

	Code Word 10								Syndrome 18			
error	d0	d1	d2	d3	c0	c1	c2	c3	s0	s1	s2	s3
none	0	0	0	0	0	0	0	0	0	0	0	0
c3	0	0	0	0	0	0	0	1	0	0	0	1
c2	0	0	0	0	0	0	1	0	0	0	1	0
c1	0	0	0	0	0	1	0	0	0	1	0	0
c0	0	0	0	0	1	0	0	0	1	0	0	0
d3	0	0	0	1	0	0	0	0	0	1	1	1
d2	0	0	1	0	0	0	0	0	1	0	1	1
d1	0	1	0	0	0	0	0	0	1	1	0	1
d0	1	0	0	0	0	0	0	0	1	1	1	0

FIG. 6C

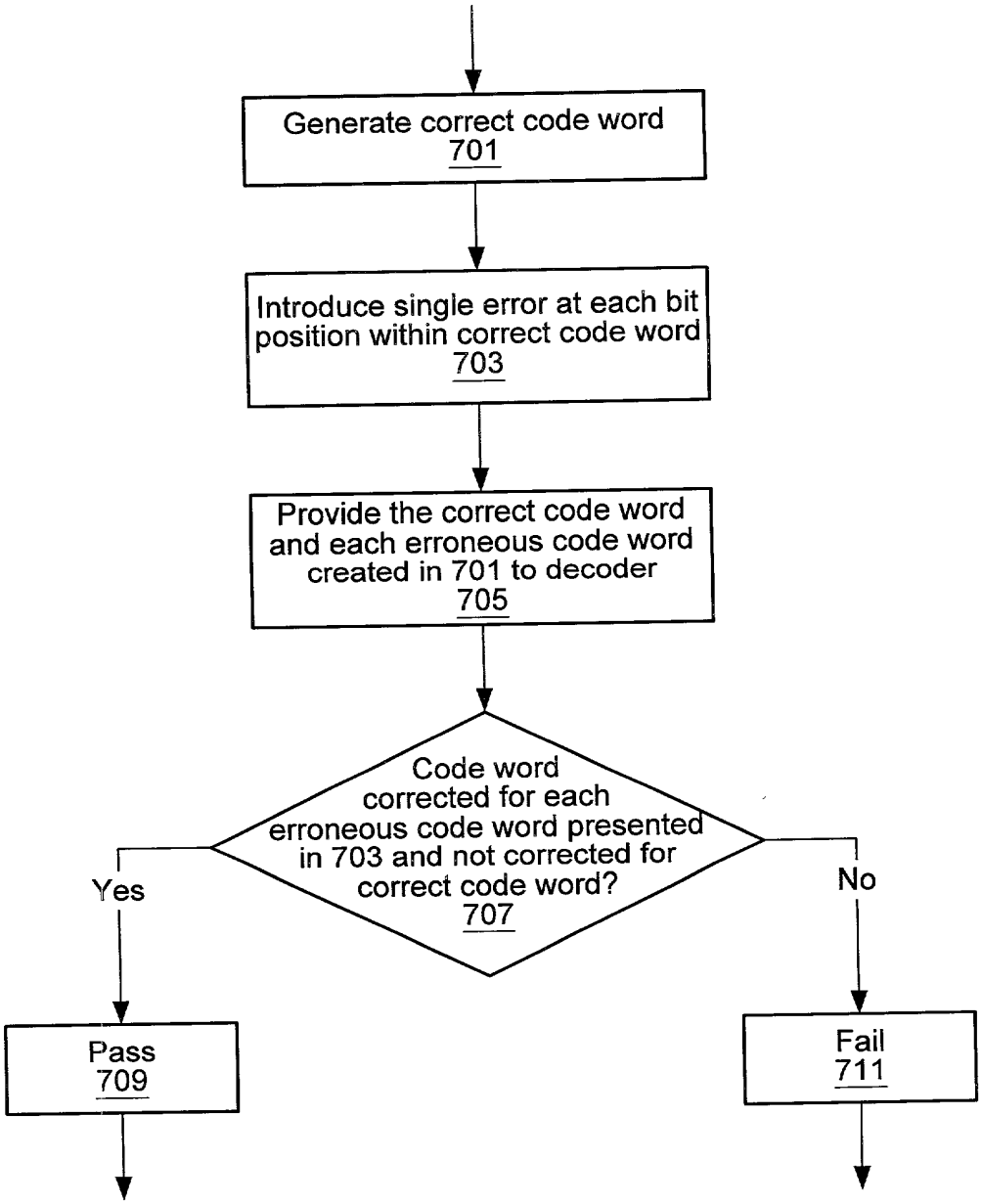

Generate correct code word
701
Introduce single error at each bit position within correct code word
703
Provide the correct code word and each erroneous code word created in 701 to decoder
705
Code word corrected for each erroneous code word presented in 703 and not corrected for correct code word?
707
Yes
No
Pass
709
Fail
711

FIG. 7

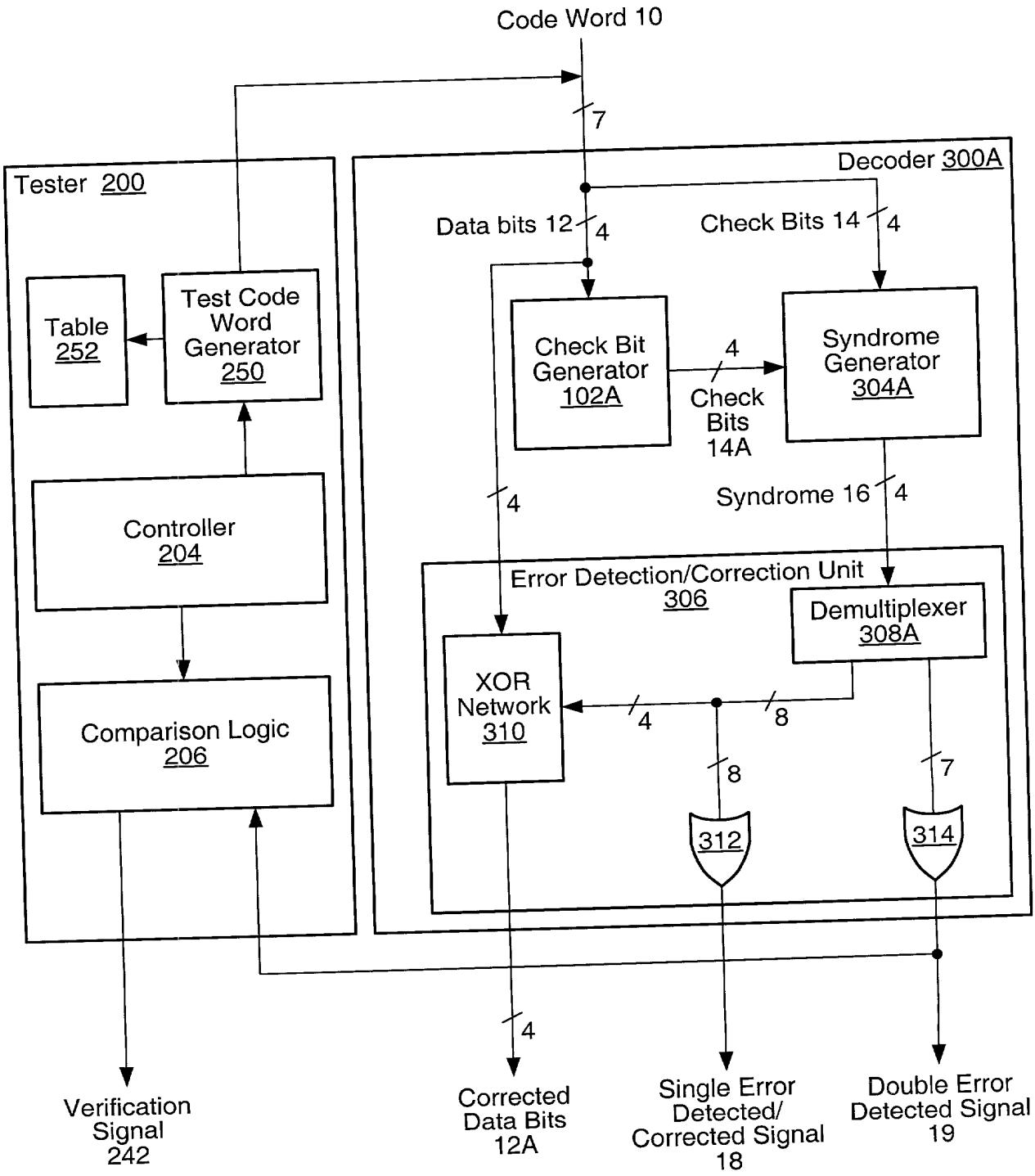

Code Word 10
7
Tester 200
Decoder 300A
Data bits 12
4
Check Bits 14
4
Table
252
Test Code
Word
Generator
250
Check Bit
Generator
102A
4
Check
Bits
14A
Syndrome
Generator
304A
Controller
204
4
Syndrome 16
4
Error Detection/Correction Unit
306
Demultiplexer
308A
XOR
Network
310
4
8
8
7
312
314
Comparison Logic
206
4
Verification
Signal
242
Corrected
Data Bits
12A
Single Error
Detected/
Corrected Signal
18
Double Error
Detected Signal
19

FIG. 8A

Table 60

Used Syndromes				Encoded Binary Value	Identified Error
0	0	0	0	0	None
0	0	0	1	1	c3
0	0	1	0	2	c2
0	1	0	0	4	c1
1	0	0	0	8	c0
0	1	1	1	7	d3
1	0	1	1	11	d2
1	1	0	1	13	d1
1	1	1	0	14	d0

Table 70

Unused Syndromes				Encoded Binary Value
0	0	1	1	3
0	1	0	1	5
0	1	1	0	6
1	0	0	1	9
1	0	1	0	10
1	1	0	0	12
1	1	1	1	15

FIG. 8B

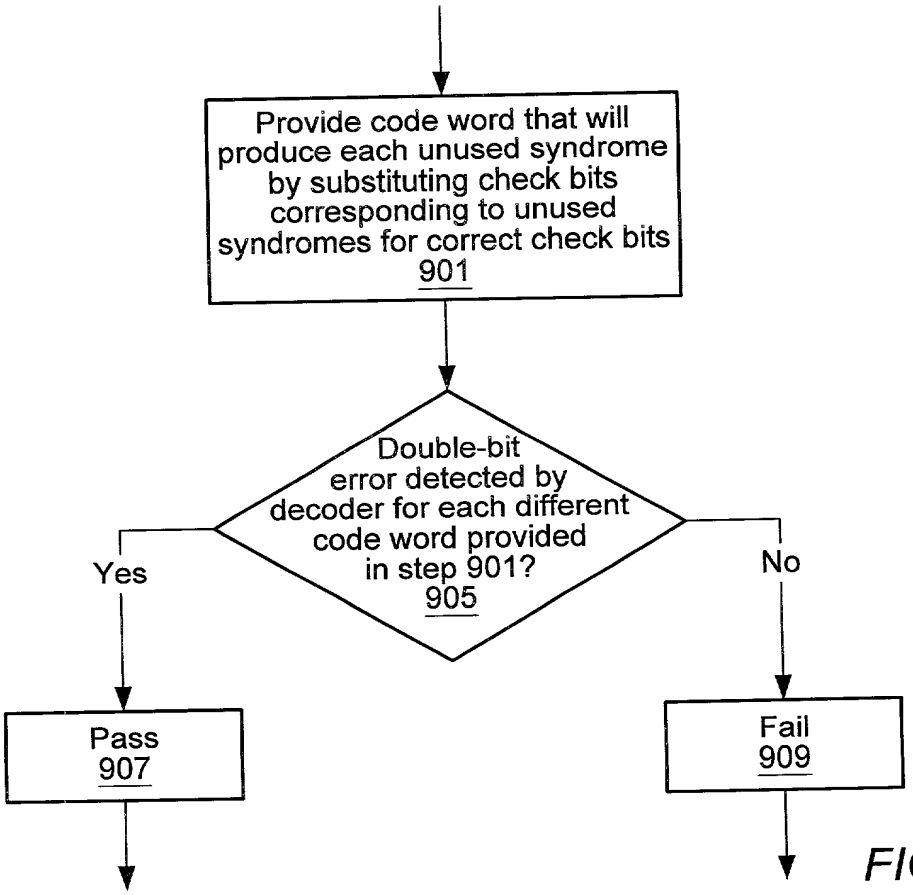

Provide code word that will produce each unused syndrome by substituting check bits corresponding to unused syndromes for correct check bits
901
Double-bit error detected by decoder for each different code word provided in step 901?
905
Yes
No
Pass
907
Fail
909

FIG. 9

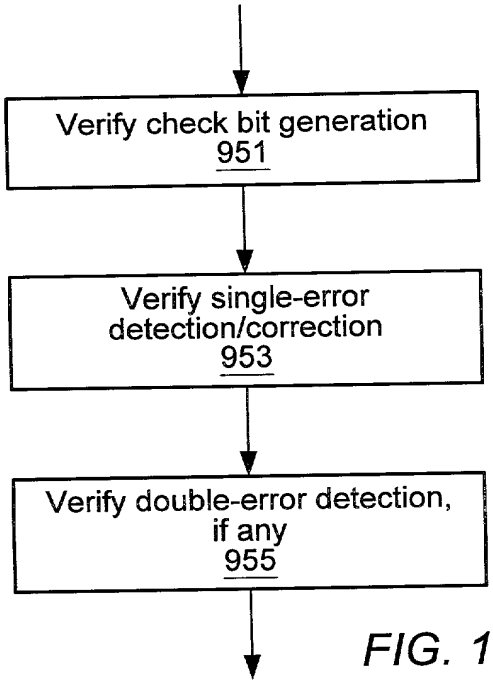

Verify check bit generation
951
Verify single-error detection/correction
953
Verify double-error detection, if any
955

FIG. 10